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(54) **Reversible connectors**

Umkehrbarer Stecker

Connecteurs réversible

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Description

Field of the Invention

[0001] The invention relates to the field of connectors, and notably to the field of connectors for computers. It notably applies to multiprocessor environments.

Background of the Invention

[0002] The number of different types of printed circuits boards used for manufacturing a computer is increasing together with the requirement for advanced performance. The number of boards attached to a computer motherboard is thus increasing. This creates several types of problems. First, the physical size of computers increases, due to the number and volume of the different boards. Second, the number and length of signal lines on the motherboard increase; this creates routing problems and crosstalk. Third, the efficient cooling of the different boards is becoming increasingly complex and difficult to carry out.

[0003] These problems are notably encountered in multiprocessor environments. Computer performance is improving by using more and more sophisticated processors at high prices and/or by using complex implementations to gain a few percentage increase of bandwidth on DRAM or communication busses. It was therefore suggested to increase the number of processors running rather than increasing processor computation speed in order to greatly improve computer performance. Such a conventional multiprocessing system requires a large package and long signal lines. Further, since the multiprocessing system comprises a plurality of CPUs, it generates a large amount of heat compared to a single processing system. A number of bus topologies are known such as DE 35 13 542A.

[0004] Figure 1 is a schematic view of such a multiprocessor system, exemplified with three different processors. The multiprocessor system of FIG. 1, comprises three processor printed circuit boards or cards 1, 2, 3, each of which includes a CPU 4, 5, 6 and a cache memory 7, 8 or 9. Each processor circuit board is connected to a common processor bus 10. The common processor bus is also connected to a memory controller 12; this controller is connected to a memory 14, e.g. a DRAM (Dynamic Random Access Memory). Each processor accesses memory 14 through the common processor bus 10 and the memory controller 12.

Summary of the Invention

[0005] Accordingly, the purpose of the invention is to provide a solution to the problems discussed above, without further complicating the structure of the different boards.

[0006] According to the invention, there is provided a bus, having:

- at least two parallel bus lines,
- at least two connectors, each connector comprising at least two bus-terminals each connected to one bus line, and at least one terminal not connected to a bus line,

wherein:

- one connector having a given pinout is the image of another connector having the same pinout in a rotation of 180 degrees,
- an image in the rotation of a bus-terminal of said one connector is a bus-terminal of said another connector, and
- a terminal of said one connector not connected to a bus line is electrically connected to the terminal of said another connector that is its image in the rotation.

[0007] Preferably, the image in the rotation of one given terminal having a given logic level is a terminal having an opposite logic level.

[0008] According to an embodiment of the invention, all terminals of a connector are on one side of the bus lines. The terminals may comprise power and ground terminals.

[0009] The invention also provides a circuit board, comprising:

- a connector with at least two connector terminals;
- switching means having connector-side terminals connected to said connector terminals, chip-side terminals, and a control input;

said switching means mapping the chip-side terminals to the connector-side terminals under control of said control input wherein the control input is preferably responsive to a signal received on a terminal on the board.

[0010] The control input is preferably connected to a connector terminal. The switching means may comprise two buffers, the terminals of each buffer being connected to the connector-side terminals and to the chip-side terminals, a signal received on said control input enabling either one of said two buffers.

[0011] The invention also covers a combination of a such computer board with a such circuit board.

[0012] The invention also provides for a computer system including a computer board with a bus having parallel bus lines and at least two identical connectors, each connector having a plurality of terminals extending generally along a first direction, and at least two identical circuit boards, each connected to one of said connectors, where one connector is the image of another connector rotated through 180 degrees about an axis that is perpendicular to the first direction, and wherein the circuit boards connected to said one connector and said another connector are relatively shifted in a direction perpendicular to the axis of rotation.

[0013] Finally, the invention provides a process for routing signals on a motherboard to at least one circuit board connected in one connector of a series of identical connectors in alternate directions, comprising the steps of:

- routing the signals along parallel bus lines to the connectors, thus changing the mapping of the terminals of the connectors to the bus lines between connectors in alternate directions;
- switching the signals received on each circuit board according to the direction of the connector, so as to have an identical mapping of the switched signals to the bus lines, whatever the direction of the connector.

[0014] The direction of a connector may be determined in a circuit board according to the polarity of a given terminal of the circuit board connector; the step of switching preferably comprises:

- storing the signals in a first buffer, in a given order;
- storing the signals in a second buffer, in a different order; and
- reading the signals from one of said first and second buffers.

Brief Description of the Drawings

[0015] A multiprocessor system embodying the invention will now be described, by way of non-limiting example, with reference to the accompanying drawings, in which

- **Figure 1** is a schematic view of a multiprocessor system;
- **Figure 2** is a front view of the multiprocessor system according to the invention;
- **Figure 3** is a view of a bus according to the invention;
- **Figure 4** is a view of a card according to the invention, in a first position;
- **Figure 5** is a view of the switching means of the card of Figure 4;
- **Figure 6** is a view of a possible connector pinout.

Best Mode of Carrying Out the Invention

[0016] Figure 2 is a front view of the multiprocessor system according to the invention; the multiprocessor system of Figure 2 comprises elements similar to those of Figure 1 and bearing the same reference numbers. The memory controller 12 is connected to the processor bus 10. Each processor circuit board 1, 2 and 3 is connected to the processor bus 10, and is arranged to be perpendicular to the processor bus.

[0017] According to the invention, and as explained below in reference to Figures 3 to 6, the circuit boards may be arranged on one side or the other of the bus; it is therefore possible, as depicted in Figure 1, to limit the space used by the different circuit boards, by arranging the boards alternately on each side of the bus. In the configuration exemplified on Figure 2, the first circuit board 1 is arranged on the right side of the processor bus, with the processor 7 facing the memory controller. Figure 2 also shows the cooling unit 21 of the processor. The second circuit board 2 is arranged on the left side of the processor bus, with the processor 8 and the cooling unit 22 facing away from the memory controller. The third circuit board 3 is arranged like the first one. Reference numeral 23 identifies the cooling unit of the processor 9 of the third circuit board. Thus, the overall space used by the processor circuit boards is limited, even though the same boards may be used. In other words, in the structure of Figure 2, the computer board comprises a bus having parallel bus lines and three identical connectors, and three identical circuit boards, each connected to one of said connectors; each connector is the image of the adjacent connector in a rotation of 180 degrees, and the circuit boards connected to the adjacent connectors are relatively shifted.

[0018] In the configuration of Figure 2, voltage regulator sockets 24, 25 and 26 for the different processor boards are arranged on alternate sides of the processor bus, on the same side as the corresponding processor circuit boards. The structure of Figure 2 has the following advantages. The distance between the successive socket assemblies on the processor bus can be reduced, the length of the bus can be shortened, and, finally, a package size of the multiprocessing system can be minimised. Furthermore, bus lines routing is straightforward, and the lines can have large line insulation, which reduces crosstalk. The CPU dedicated voltage regulators can be provided very close to each CPU, and consequently, signal line length between each CPU and each CPU dedicated voltage regulator can be reduced. Therefore, the voltage drop between the two can be reduced. Furthermore, the successive circuit boards constitute channels for airflow, so that the cooling of the different processors and voltage regulators is more efficient.

[0019] The staggered structure described in reference to Figure 2 may be used not only for processor boards, but for any type of boards. It is particularly useful for boards that have significant thickness on part of their surface - such as processor boards, which have a cooling unit installed on the processor.

[0020] Figure 3 is a view of a bus assembly according to the invention. The bus of Figure 3 comprise a series of bus lines 30_1 to 30_n, where n is the number of bus lines, e.g. n=64 in a usual computer configuration. These lines are parallel and are connected to a controller 32. The bus also comprises a series of connectors 34_1 to 34_m, where m is the number of connectors, e.g. m=4 for a multiprocessor configuration. The different connectors have the same pinout; however, a given con-

nector 34_i is rotated through 180 degrees with respect to an adjacent connector 34_{i+1}. Figure 3 shows the centre of rotation A of the rotation that transforms connector 34_2 into connector 34_3 (and vice-versa). All connectors have the same pinout, and comprise a polarising key 35_i that mechanically distinguishes the direction of a connector.

[0021] Each connector comprises a series of bus-sockets $36_{i,j}$, where $1 \le i \le m$ and $1 \le j \le n$, each of which is connected to a different bus line. Each connector also comprises a series of sockets $38_{i,k}$, where $1 \le i \le m$ and $1 \le j \le p$, that are not connected to a bus line. These sockets may for instance comprise power supply sockets, ground sockets, identifying sockets for identifying each connector, a reset socket for separately resetting a card connected to a given connector, etc. These sockets may be arranged as shown in Figure 3 on one side of the bus lines; they may also be arranged on both sides of the bus lines, according to the needs.

[0022] According to the invention, an image in the rotation of a bus-socket of one connector is a bus-socket of the adjacent connector. In other words, the image in the rotation of the assembly $\{36_{i,j}, 1 \le j \le n\}$ of all bus-sockets of connector i is the assembly $\{36_{i+1,k}, 1 \le k \le n\}$ of all bus-sockets of connector i+1. Since there is only one invariant point in a rotation, this means that there exists at least one bus-socket connected to a given bus line, the image of which is not connected to the same bus line. In the case depicted in Figure 3, the image in the rotation of bus-socket $36_{i,j}$ is bus socket $36_{i+1,n+1-j}$: the image of a bus socket connected to a given bus line is therefore a bus-socket connected to a different bus-line.

[0023] On the other hand, a socket $38_{i,k}$ that is not connected to a bus line, and its image the image $38_{i+1,k}$ may very well be electrically connected, that is may have the same function, or be connected to the same line or plane of the board. This is indeed possible, since there is no constraint that the lines between all sockets not connected to the bus lines and their respective images be parallel.

[0024] In other words, according to the invention, in the rotation that transforms connector i into connector i + 1:

- each bus-socket is transformed into a bus socket connected to a different bus line;
- each socket not connected to a bus line is transformed into a socket, to which it is electrically connected.

This means that the bus lines are parallel, and that the lines connecting the other sockets to their respective images are not parallel.

[0025] The bus described in reference to Figure 3 is adapted to provide the structure described in reference to Figure 2, with the cards or circuit boards described below. Figure 4 is a view of a card according to the invention; such a card comprises a connector adapted to be connected to a bus connector; in the exemplified embodiment, the connector 40 is a pin connector adapted to be connected to the socket connector of Figure 3. Connector 40 thus comprises n+p pins, and a recess 42 corresponding to the polarising key 35 of the socket connector. Out of the n+p pins, n bus pins, say bus pins 44_h, $1 \le h \le n$ are connected to the bus sockets 36 when the connector 40 is connected to the socket connector. The p other pins, say pins 46_h, $1 \le h \le p$ are connected to the sockets 38 when the connector 40 is connected to the socket connector.

[0026] The card of Figure 4 may be connected to any one of the socket connectors of Figure 3, and thus, one given bus pin 44_h, $1 \le i \le n$ may be connected to different bus lines, according to the socket connector in which the card is inserted. In the example of Figure 3, bus pin 44_h would be connected to bus socket 36_h, and thus to bus line 30_h or 30_{n+1-h}, according to the socket connector. On the other hand, the pins 46_h, $1 \le i \le p$ of the card are connected to the same logical or electrical signal, whatever the connector into which the card is plugged.

[0027] In order to ensure proper operation of the card, whatever the socket connector into which it is plugged, the card comprises also switching means 48. The connector-side terminals 50_h of the switching means are connected to the bus pins 42_h of the connector, and the chip-side terminals 52_h of the switching means 48 provide signals that may be used in the card, e.g. in a microprocessor chip . The switching means ensure that whatever the connector into which the card is plugged, the chip-side terminals of the switching means are correctly mapped to the bus lines. In other words, the switching means ensure that for any value h, $1 \le h \le n$, the chip-side terminal 52_h of the switching means 48 are connected or mapped on the bus line 30_h.

[0028] Thus, the card according to the invention may be plugged in any connector of the bus described in reference to Figure 3: the switching means will in any case ensure a correct mapping of the chip terminals to the bus lines.

[0029] In the example given above, in a first connector 34_i, socket 36_j is connected to bus line 30_j; socket 36_j is connected to bus pin 44_j, that is connected to connector-side terminal 50_j; the switching means ensure that chip-side terminal 52_j is directly connected to connector-side terminal 50_j. On the other hand, in a connector 34_{i+1} arranged in the opposite direction, 36_j is connected to bus line 30_{n+1-j}; socket 36_j is connected to bus pin 44_j, that is connected to connector-side terminal 50_j; the switching means ensure that chip-side terminal 52_{n+1-j} is connected to connector-side terminal 50_j. Thus, chip-side terminal 52_{n+1-j} is correctly mapped to bus line 30_{n+1-j}.

[0030] Switching means may be embodied and controlled in a plurality of ways. Figure 5 is a view of a possible embodiment of the switching means. The switching means are controlled by the signal received on a given pin of the connector 40, say pin 46_q. Sockets 38_q and 38_{n+1-q} are respectively connected to opposite logical

levels, say level "0" for socket 38_q, and level "1" for socket 38_{n+1-q}. In the case of a connector in a first direction, say connector 34_1 in the example of Figure 3, pin 46_q is connected to socket 38_q, that is to "0"; thus, the switching means 48 receive a control signal that is a logical "0". In the case of a connector in the opposite direction, say connector 34_2 in the example of Figure 3, pin 46_q is connected to socket 38_{n+1-q}; thus, the switching means 48 receive a control signal that is a logical "1". This clearly makes it possible to command the switching means, according to the direction of the connector into which the card is plugged. Obviously, the switching means may be integrated in a chip, if necessary.

[0031] Figure 5 simply shows how the switching means may, under control of the signal received on pin 46_q, switch the connector-side terminal 50_h either to chip-side terminal 52_h or to chip-side terminal 52_{n+1-h}, and respectively, terminal 50_{n+1-h} either to chip-side terminal 52_{n+1-h} or to chip-side terminal 52_h As depicted on Figure 5, pin connector 44_h is connected to connector-side terminal 50_h, and pin connector 44_{n+1-h} is connected to connector-side terminal 50_{n+1-h}. The control signal received on pin 46_q is transmitted to a control input terminal 54. The signal received on control input terminal 54 is provided to an inverter 56.

[0032] The signal received on connector-side terminal 50_h (respectively 50_{n+1-h}) is provided to two buffers 58_h and 60_h (respectively 58_{n+1-h} and 60_{n+1-h}). The outputs of buffers 58_h and 60_{n+1-h} are connected to chip-side terminal 52_h; the outputs of buffers 58_{n+1-h} and 60_h are connected to chip-side terminal 52_{n+1-h}. Buffers 58_h and 58_{n+1-h} are enabled by the signal provided on control input terminal 54, whereas buffers 60_h and 60_{n+1-h} are enabled by the signal output by inverter 56. The operation of the switching means of Figure 5 is clear.

[0033] In the embodiment of Figure 5, the switching means are operating in one direction only. They may be duplicated in order to ensure routing of the signals to and from the card; one may also provide other embodiments, e.g. a bidirectional buffer, or a switch. In the embodiment of Figure 5, the signals of two sockets are used in order to control the switching means; there are other ways to control the switching means, e.g. two different pins of the connector 40 may be used, one pin only being connected to a given logical level, according to the direction of the connector.

[0034] Figure 6 is a view of a possible connector pinout, according to the invention. Figure 6 shows the bus lines 30_1 to 30_{16}, a first card connector 62, with a control pin 64, corresponding to pinout 46_1, and a second connector 66, with a control pin 68 , corresponding to pinout 46_1. As shown on Figure 6, control pin 64 is connected to VCC, whereas control pin 68 is connected to ground, so as to ensure a correct mapping of the chip-side terminal of the switching means to the bus lines.

[0035] It is clear that the scope of invention not only covers the example described in reference to Figure 3, where each connector is the image of an adjacent connector after a rotation through 180 degrees, but also other configurations, where some of the connectors are arranged in the same direction as the adjacent connectors: it is sufficient that at least one connector is the image of an adjacent connector in a rotation of 180 degrees. For instance, the scope of the invention covers the configuration where two connectors are arranged on one side of the bus lines, and where the two next connectors are arranged on the other side of the bus lines. It is also not necessary that all connectors have exactly the same pinout. One could imagine that two different types of connectors are provided on a given bus. The invention is also not limited to the exemplified pinout of the preferred embodiments described above.

[0036] Also, the invention was described above in the usual configuration where the bus connectors are socket connectors, and the circuit boards connectors are pin connector. It should be understood that the invention is not limited to this configuration, and that the usual types of edge connectors provided in the computer industry may also be used. The words "connector terminal" thus notably cover pins, sockets, edge lands and spring terminals adapted to mate with such lands.

[0037] Furthermore, it is clear for the person skilled in the art that the bus lines of the invention are parallel in that they do not intersect. This is the proper meaning in the invention of the word parallel; it is not necessary that the bus lines are "parallel" in the mathematical meaning of this word to ensure the advantages of the invention.

Claims

1. A bus, having:

   - at least two parallel bus lines (30_i),
   - at least a first and a second connector (34_i) having the same pinout, each connector comprising at least two bus-terminals ($36_{i,j}$) each connected to one bus line, and at least one non-bus terminal ($38_{i,j}$) not connected to a bus line,

   characterised in that the first connector (34_i) is the image rotated through 180 degrees of the second connector (34_{i+1}) with this image rotation mapping each bus terminal of the second connector to a respective bus terminal of the first connector, and mapping a predetermined non-bus terminal of the second connector to a predetermined non-bus terminal of the first connector, said predetermined non-bus terminals being electrically connected to each other.

2. A bus according to claim 1, wherein the image in the rotation of one given terminal having a given logic level is a terminal having an opposite logic level.

3. A bus according to claim 1 or 2, wherein all termi-

nals of a connector are on one side of the bus lines.

4. A computer board comprising a bus according to one of claims 1 to 3, said at least on non-bus terminal of each connector comprising power and ground terminals.

5. A circuit board, comprising:

   - a connector (40) with at least two connector terminals (44_h ,46_h);
   - switching means (48) having connector-side terminals (50_h) connected to said connector terminals (44_h), chip-side terminals (52_h),

   characterised in that said switching means has a control input (54);
   said switching means mapping the chip-side terminals (52_h) to the connector-side terminals (50_h) under control of said control input wherein the control input is responsive to a signal received on a connector terminal on the board.

6. A circuit board according to claim 5, wherein said control input is connected to a connector terminal (46_h).

7. A circuit board according to claim 5 or 6, wherein said switching means comprise two buffers (60_h, 62_h), the terminals of each buffer being connected to the connector-side terminals (50_h) and to the chip-side terminals (52_h), a signal received on said control input enabling either one of said two buffers.

8. A combination of a computer board according to claim 4 with a circuit board according to claim 5, 6 or 7.

9. A computer system including a computer board with a bus having parallel bus lines and at least two identical connectors, each connector having a plurality of terminals extending generally along a first direction, and at least two identical circuit boards, each connected to one of said connectors, where the circuit boards connected to said one connector and said another connector are relatively shifted in a direction perpendicular to the axis of rotation, **characterised in that** one connector is the image of another connector rotated through 180 degrees about an axis that is perpendicular to the first direction.

10. A process for routing signals on a motherboard to at least one circuit board connected in one connector (34_i) of a series of identical connectors in alternate directions, comprising the steps of:

    - routing the signals along parallel bus lines (30_i) to the connectors (34_i), thus changing the mapping of the terminals of the connectors to the bus lines between connectors in alternate directions;
    - switching the signals received on each circuit board according to the direction of the connector, so as to have an identical mapping of the switched signals to the bus lines, whatever the direction of the connector.

11. A process according to claim 10, wherein the direction of a connector is determined in a circuit board according to the polarity of a given terminal of the circuit board connector.

12. A process according to claim 10 or 11, wherein the step of switching comprises:

    - storing the signals in a first buffer (60_h), in a given order;
    - storing the signals in a second buffer (62_h), in a different order; and
    - reading the signals from one of said first and second buffers.

Patentansprüche

1. Ein Bus mit folgenden Merkmalen:

   zumindest zwei parallelen Busleitungen (30_i),

   zumindest einem ersten und einem zweiten Verbindungselement (34_i), die den gleichen Außenanschluß haben, wobei jedes Verbindungselement zumindest zwei Busanschlüsse ($36_{i,j}$), die jeweils mit einer Busleitung verbunden sind, sowie zumindest einen Nicht-Bus-Anschluß ($38_{i,j}$) aufweist, der mit keiner Busleitung verbunden ist,

   dadurch gekennzeichnet, daß das erste Verbindungselement (34_i) das Bild des zweiten Verbindungselementes (34_{i+1}) ist, das um 180° gedreht ist, wobei diese Bilddrehung jeden Busanschluß des zweiten Verbindungselementes auf einen jeweiligen Busanschluß des ersten Verbindungselementes abbildet und einen vorbestimmten Nicht-Bus-Anschluß des zweiten Verbindungselementes auf einen vorbestimmten Nicht-Bus-Anschluß des ersten Verbindungselementes abbildet, wobei die vorbestimmten Nicht-Bus-Anschlüsse elektrisch miteinander verbunden sind.

2. Ein Bus gemäß Anspruch 1, bei dem das Bild, in der Drehung, eines bestimmten Anschlusses, der einen bestimmten Logikpegel aufweist, ein Anschluß ist, der einen entgegengesetzten Logikpegel aufweist.

3. Ein Bus gemäß Anspruch 1 oder 2, bei dem alle Anschlüsse eines Verbindungselementes auf einer Seite der Busleitungen sind.

4. Eine Computerplatine, die einen Bus gemäß einem der Ansprüche 1 bis 3 aufweist, wobei der zumindest eine Nicht-Bus-Anschluß jedes Verbindungselementes einen Leistungs- und einen Masseanschluß aufweist.

5. Eine Schaltungsplatine mit folgenden Merkmalen:

einem Verbindungselement (40) mit zumindest zwei Verbindungselementanschlüssen (44_h, 46_h);

einer Schalteinrichtung (48), die verbindungselementseitige Anschlüsse (50_h), die mit den Verbindungselementanschlüssen (44_h) verbunden sind, und chipseitige Anschlüsse (52_h) aufweist,

dadurch gekennzeichnet, daß die Schalteinrichtung einen Steuerungseingang (54) aufweist, wobei die Schalteinrichtung die chipseitigen Anschlüsse (52_h) unter der Steuerung des Steuerungseingangs auf die verbindungselementseitigen Anschlüsse (50_h) abbildet, wobei der Steuerungseingang ansprechend auf ein Signal ist, das an einem Verbindungselementanschluß auf der Platine empfangen wird.

6. Eine Schaltungsplatine gemäß Anspruch 5, bei der der Steuerungseingang mit einem Verbindungselementanschluß (46_h) verbunden ist.

7. Eine Schaltungsplatine gemäß Anspruch 5 oder 6, bei der die Schalteinrichtung zwei Puffer (60_h, 62_h) aufweist, wobei die Anschlüsse jedes Puffers mit den verbindungselementseitigen Anschlüssen (50_h) und den chipseitigen Anschlüssen (52_h) verbunden sind, und wobei ein Signal, das an dem Steuerungseingang empfangen wird, einen der beiden Puffer aktiviert.

8. Eine Kombination einer Computerplatine gemäß Anspruch 4 mit einer Schaltungsplatine gemäß einem der Ansprüche 5 bis 7.

9. Ein Computersystem, das eine Computerplatine mit einem Bus, der parallele Busleitungen aufweist, und zumindest zwei identischen Verbindungselementen, wobei jedes Verbindungselement eine Mehrzahl von Anschlüssen aufweist, die sich allgemein entlang einer ersten Richtung erstrecken, und zumindest zwei identische Schaltungsplatinen umfaßt, wobei jede derselben mit einem der Verbindungselemente verbunden ist, wobei die Schaltungsplatinen, die mit dem einen Verbindungselement und dem anderen Verbindungselement verbunden sind, relativ in eine Richtung senkrecht zu der Drehachse verschoben sind, **dadurch gekennzeichnet, daß** ein Verbindungselement das Bild eines anderen Verbindungselementes ist, das um 180° um eine Achse gedreht ist, die senkrecht zu der ersten Richtung ist.

10. Ein Verfahren zum Leiten von Signalen auf einer Hauptplatine zu zumindest einer Schaltungsplatine, die in einem Verbindungselement (34_i) einer Serie identischer Verbindungselemente in abwechselnden Richtungen verbunden ist, mit folgenden Schritten:

Leiten der Signale entlang paralleler Busleitungen (30_i) zu den Verbindungselementen (34_i), wobei so die Abbildung der Anschlüsse der Verbindungselemente auf die Busleitungen zwischen Verbindungselementen in abwechselnden Richtungen verändert wird;

Schalten der Signale, die auf jeder Schaltungsplatine empfangen werden, gemäß der Richtung des Verbindungselementes, um so unabhängig von der Richtung des Verbindungselementes eine identische Abbildung der geschalteten Signale auf die Busleitungen zu haben.

11. Ein Verfahren gemäß Anspruch 10, bei dem die Richtung eines Verbindungselementes in einer Schaltungsplatine gemäß der Polarität eines bestimmten Anschlusses des Schaltungsplatinenverbindungselementes bestimmt wird.

12. Ein Verfahren gemäß Anspruch 10 oder 11, bei dem der Schritt des Schaltens folgende Schritte aufweist:

Speichern der Signale in einer bestimmten Reihenfolge in einem ersten Puffer (60_h);

Speichern der Signale in einer unterschiedlichen Reihenfolge in einem zweiten Puffer (62_h); und

Lesen der Signale von dem ersten und dem zweiten Puffer.

Revendications

1. Bus, comprenant :

- au moins deux lignes de bus parallèles (30_i) ;
- au moins un premier et un deuxième connecteurs (34_i) ayant le même brochage, chaque

connecteur comprenant au moins deux bornes de bus (36_{ij}) connectées chacune à une ligne de bus et au moins une borne de non-bus (38_{ij}) non connectée à une ligne de bus,

caractérisé en ce que le premier connecteur (34_i) est l'image retournée de 180 degrés du deuxième connecteur (34_{i+1}), cette rotation d'image mappant chaque borne de bus du deuxième connecteur vers une borne de bus respective du premier connecteur et mappant une borne de non-bus prédéterminée du deuxième connecteur vers une borne de non-bus prédéterminée du premier connecteur, lesdites bornes de non-bus prédéterminées étant connectées électriquement les unes aux autres.

2. Bus selon la revendication 1, dans lequel l'image dans la rotation d'une borne donnée ayant un niveau logique donné est une borne ayant un niveau logique opposé.

3. Bus selon la revendication 1 ou 2, dans lequel toutes les bornes d'un connecteur sont d'un côté des lignes de bus.

4. Carte informatique comprenant un bus celon l'une des revendications 1 à 3, ladite au moins une borne de non-bus de chaque connecteur comprenant des bornes de puissance et de masse.

5. Carte de circuit, comprenant :

- un connecteur (40) avec au moins deux bornes de connecteur (44_h, 46_h) ;
- des moyens de commutation (48) comportant des bornes côté connecteur (50_h) connectées auxdites bornes de connecteur (44_h), des bornes côté puce (52_h),

caractérisée en ce que lesdits moyens de commutation comportent une entrée de commande (54) ; lesdite moyens de commutation mappant les bornes côté bus (52_h) vers les bornes côté connecteur (50_h) sous la commande de ladite entrée de commande, dans laquelle l'entrée de commande est sensible à un signal reçu sur une borne de connecteur de la carte.

6. Carte de circuit selon la revendication 5, dans laquelle ladite entrée de commande est connectée à une borne de connecteur (46_h).

7. Carte de circuit selon la revendication 5 ou 6, dans laquelle lesdits moyens de commutation comprennent deux mémoires tampon (60_h, 62_h), les bornes de chaque mémoire tampon étant connectées aux bornes côté connecteur (50_h) et aux bornes côté bus (52_h), un signal reçu sur ladite entrée de commande validant l'une ou l'autre desdites mémoires tampon.

8. Combinaison d'une carte informatique selon la revendication 4 et d'une carte de circuit selon la revendication 5, 6 ou 7.

9. Système informatique comprenant une carte informatique avec un bus comportant des lignes de bus parallèles et au moins deux connecteurs identiques, chaque connecteur comportant une pluralité de bornes s'étendant généralement dans une première direction et au moins deux cartes de circuit identiques, connectées chacune à l'un desdits connecteurs, dans lequel les cartes de circuit connectées audit un connecteur et audit autre connecteur sont décalées de manière relative dans une direction perpendiculaire à l'axe de rotation, **caractérisé en ce qu'**un connecteur est l'image d'un autre connecteur tournée de 180 degrés autour d'un axe qui est perpendiculaire à la première direction.

10. Procédé pour acheminer des signaux sur une carte mère vers au moins une carte de circuit connectée à un connecteur (34_i) d'une série de connecteurs identiques dans des directions alternées, comprenant les étapes consistant à :

- acheminer les signaux le long de lignes de bus parallèles (30_i) vers les connecteurs (34_i), modifiant ainsi le mappage des bornes des connecteurs vers les lignes de bus entre les connecteurs dans des directions alternées ;
- commuter les signaux reçus sur chaque carte de circuit conformément à la direction du connecteur, de manière à avoir un mappage identique des signaux commutés vers les lignes de bus, quelle que soit la direction du connecteur.

11. Procédé selon la revendication 10, dans lequel la direction d'un connecteur est déterminée sur une carte de circuit conformément à la polarité d'une borne donnée du connecteur de carte de circuit.

12. Procédé selon la revendication 10 ou 11, dans lequel l'étape de commutation comprend :

- la mémorisation des signaux dans une première mémoire tampon (60_h), dans un ordre donné ;
- la mémorisation des signaux dans une deuxième mémoire tampon (62_h), dans un ordre différent ; et
- la lecture des signaux à partir d'une desdites première et deuxième mémoires tampon.

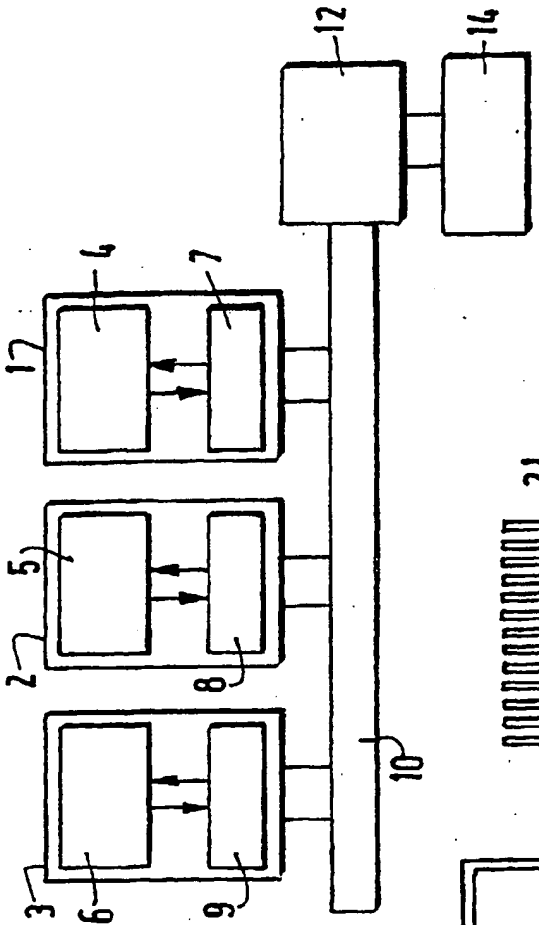

FIG.1

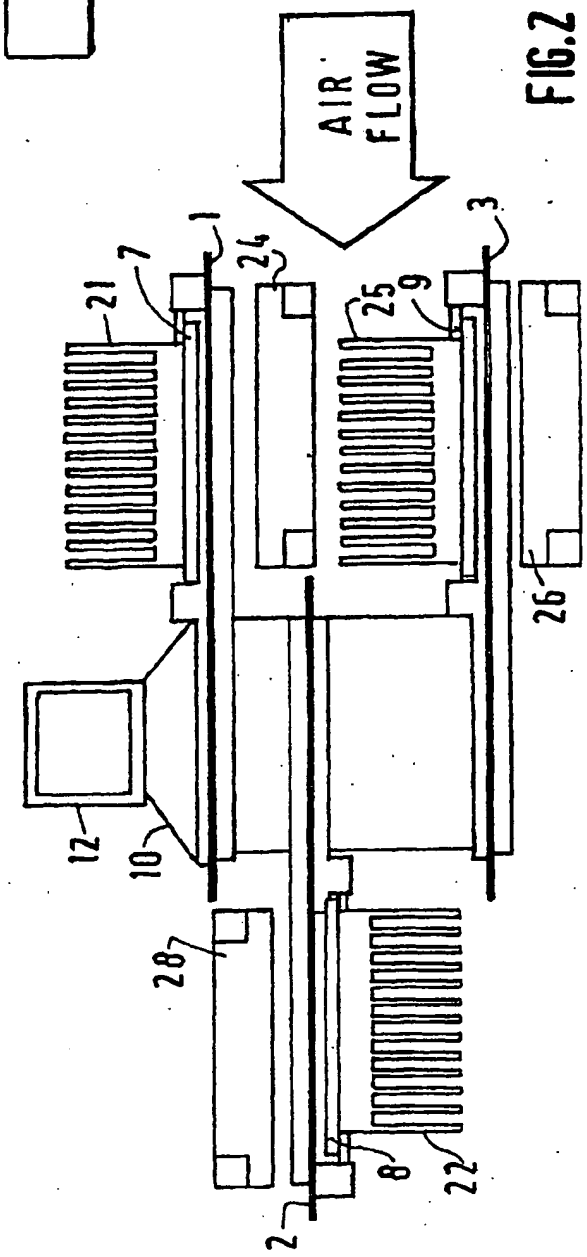

FIG.2

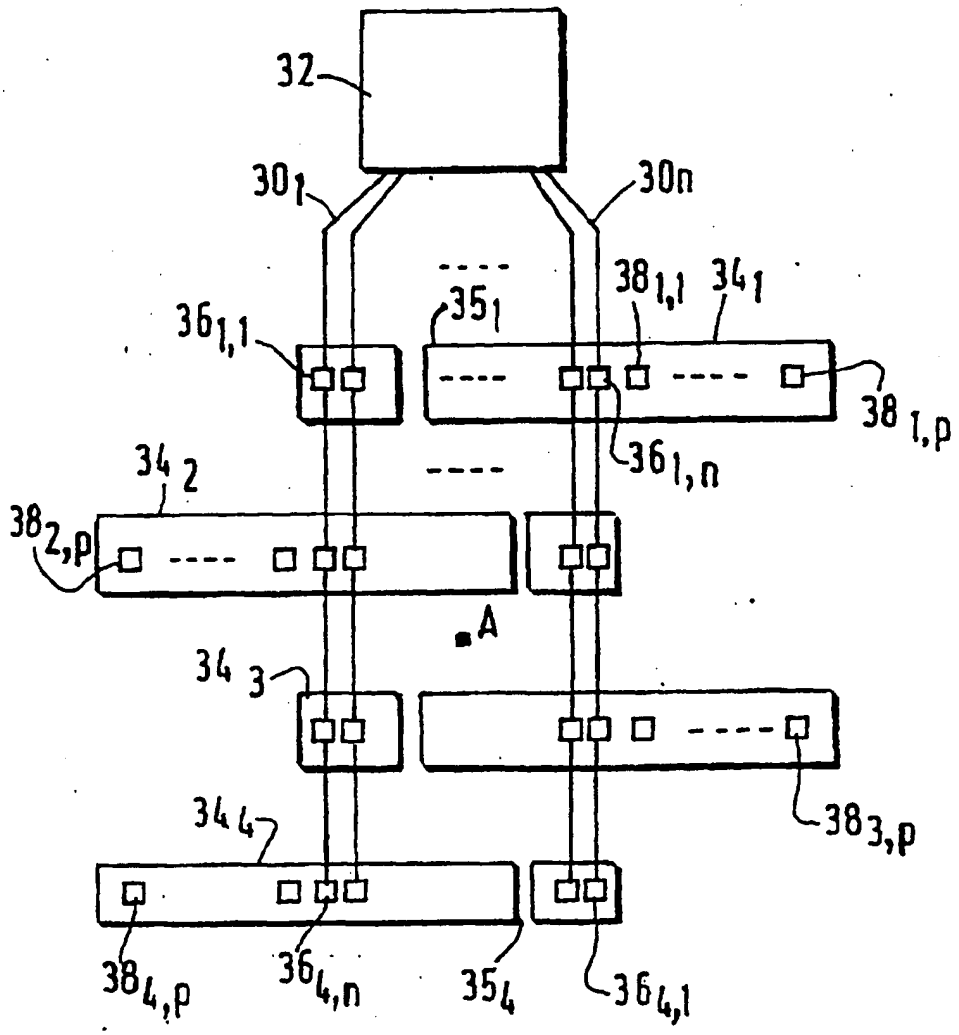
32
30 1
30n
35 1
38 1,1
34 1
36 1,1
38 1,p
36 1,n
34 2
38 2,p
A
34 3
38 3,p
34 4
38 4,p
36 4,n
35 4
36 4,1

FIG.3

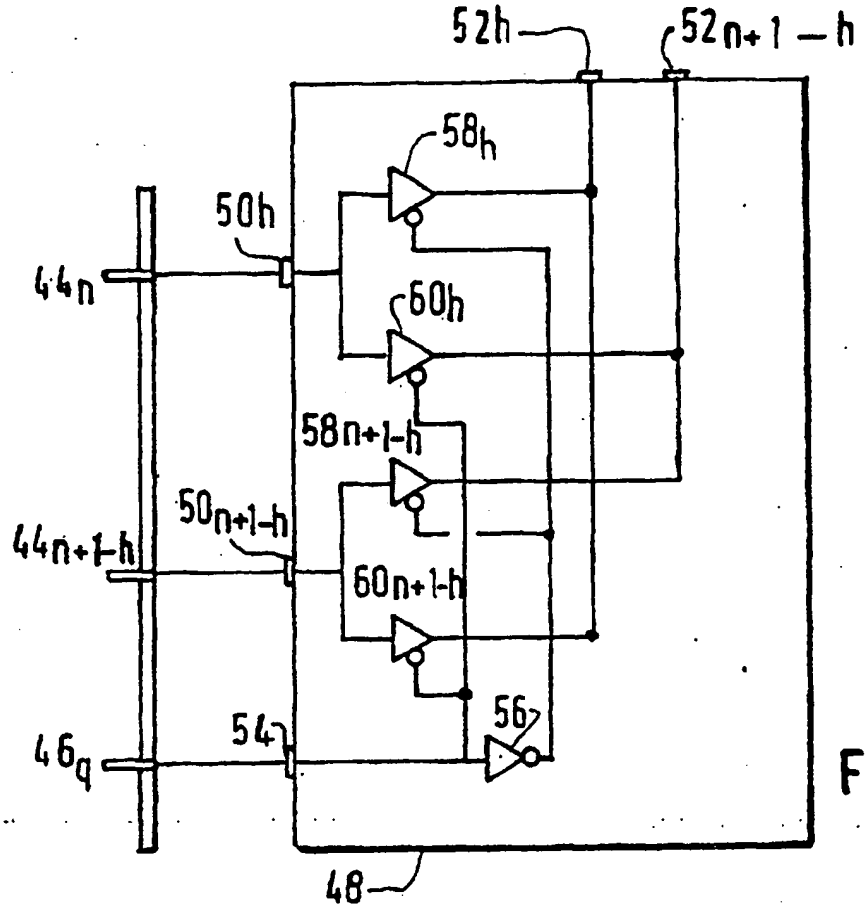
52h
52n+1−h
58h
50h
44n
60h
58n+1-h
50n+1-h
44n+1-h
60n+1-h
56
54
46q
48

FIG.5

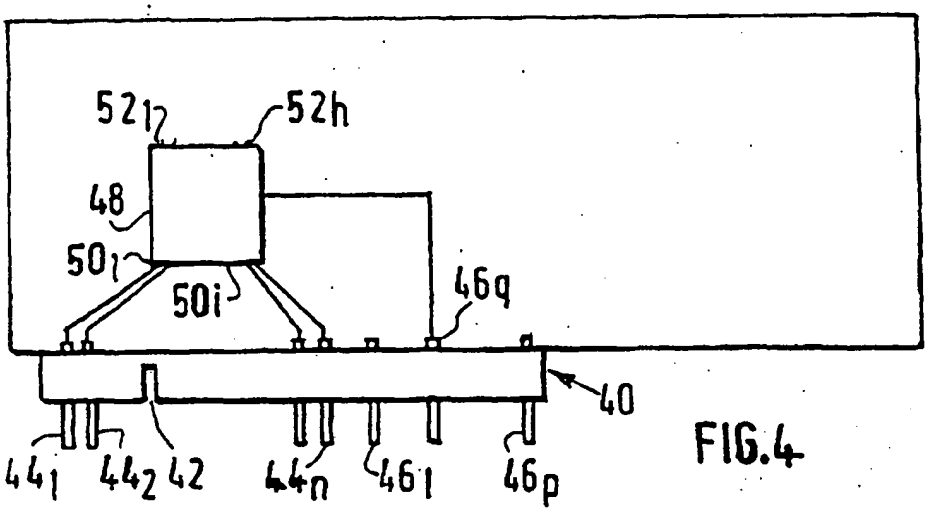
521
52h
48
501
50i
46q
40
441
442
42
44n
461
46p

FIG.4

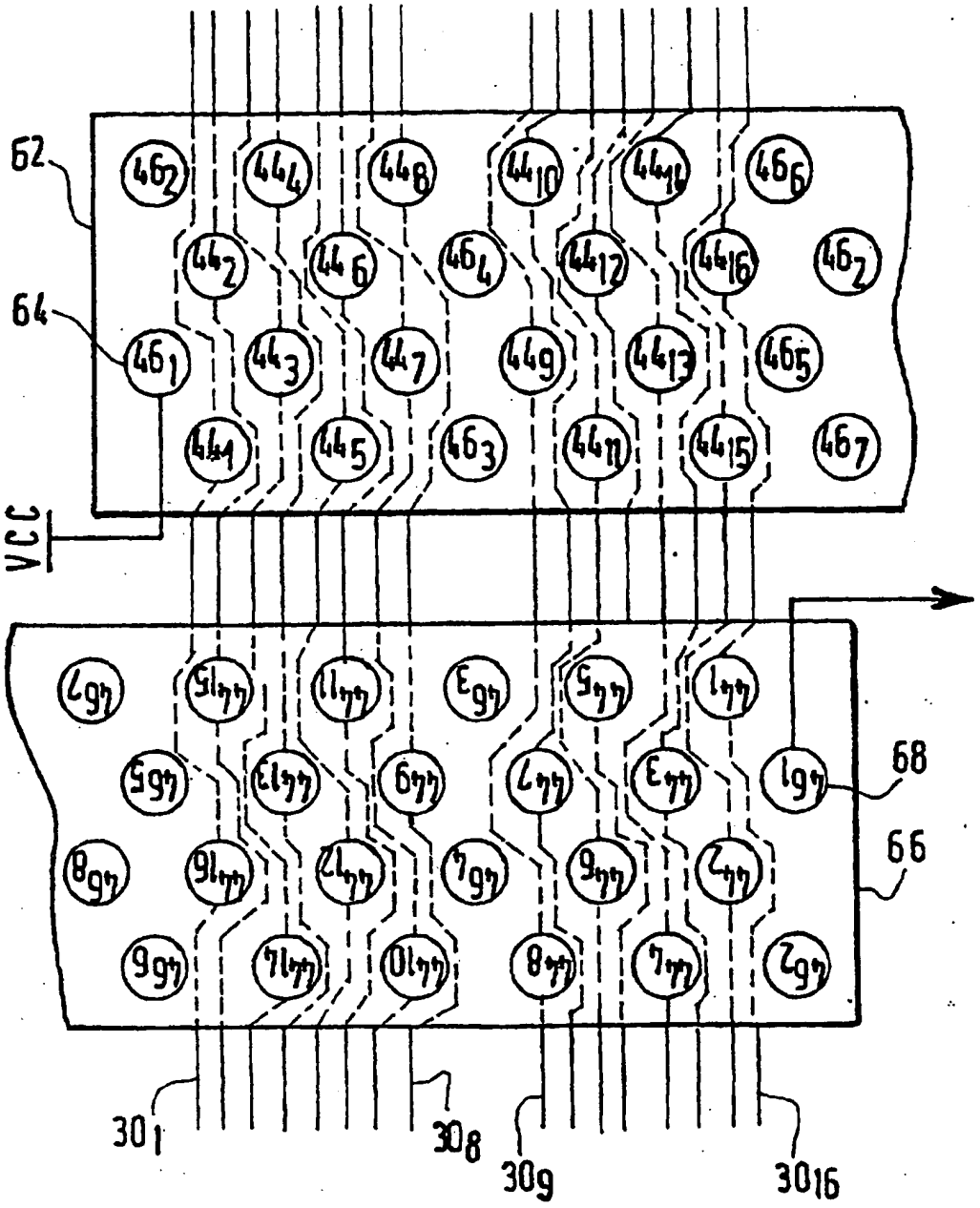

FIG. 6